	FORM PTO-1449 U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO. IMEC92.001DV1	APPLICATION NO. 10/766,159
	INFORMATION DISCLOSURE STATEMENT BY APPLICANT		
	FILING DATE January 27, 2004		GROUP Unknown

(USE SEVERAL SHEETS IF NECESSARY)

## U.S. PATENT DOCUMENTS

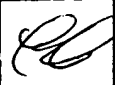
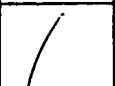
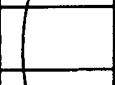
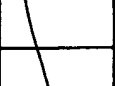
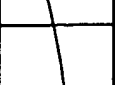
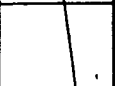
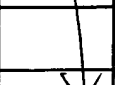
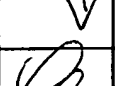
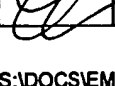
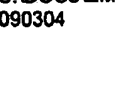
EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE (IF APPROPRIATE)
<i>MA</i>	5,978,509	11/02/99	Nachtergaele et al.	—	—	

EXAMINER INITIAL	OTHER DOCUMENTS (INCLUDING AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.)					
<i>MA</i>	2	Agarwal, R. et al., Coding of moving pictures and audio, N1693 "International organization for standardization, ISO/IEC/JTC1/SC29WG11," April 1997.				
	3	Amarasinghe, S. et al., "The SUIF compiler for scalable parallel machines," in <i>Proc. of the 7th SIAM Conf. on Parallel Proc. for Scientific Computing</i> , 1995.				
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	5	Brodersen, R.W., "The Network Computer and its Future," <i>Proc. IEEE Int. Solid-State Circ. Conf.</i> , San Francisco CA, pp.32-36, Feb. 1997.				
	6	Cathoor, F. "Energy-delay efficient data storage and transfer architectures: circuit technology versus design methodology solutions," <i>Proceedings of DATE'98</i> , Feb.23-25 1998.				
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	10	De Greef, E. et al., "Memory organization for video algorithms on programmable signal processors," <i>Proc. IEEE Int. Conf. on Computer Design</i> , Austin TX, pp.552-557, Oct. 1995.				
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	14	Kolson, D. et al., "Minimization of memory traffic in high-level synthesis," <i>Proc. 31st ACM/IEEE Design Automation Conf.</i> , San Diego CA, pp.149-154, June 1994.				
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<i>MA</i>	18	Nachtergaele, L. et al., "Low power data transfer and storage exploration for H.263 video decoder system," accepted for special issue on <i>Very low-bit rate video coding</i> (eds. Argy Krikelis et al.) of <i>IEEE Journal on Selected Areas in Communications</i> , Vol.16, No.2, Feb. 1998.				

EXAMINER	DATE CONSIDERED
<i>[Signature]</i>	9/20/04

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FORM 100-1449 U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE INFORMATION DISCLOSURE STATEMENT BY APPLICANT (USE SEVERAL SHEETS IF NECESSARY)	ATTY. DOCKET NO. IMEC92.001DV1	APPLICATION NO. 10/766,159
	APPLICANT Brockmeyer, et al.	
	FILING DATE January 27, 2004	GROUP Unknown

EXAMINER INITIAL	OTHER DOCUMENTS (INCLUDING AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.)
	19 Nachtergaele, L. et al., "Optimisation of memory organisation and hierarchy for decreased size and power in video and image processing systems," <i>Proc. Intl. Workshop on Memory Technology, Design and Testing</i> , San Jose CA, pp.82-87, Aug. 1995.
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	26 van Swaaij, M. et al., "Modelling data and control flow for high-level memory management," <i>Proc. 3rd ACM/IEEE Europ. Design Automation Conf.</i> , Brussels, Belgium, pp.8-13, March 1992.
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	28 Wolf, M. et al., "A loop transformation theory and an algorithm to maximize parallelism," <i>IEEE Trans. on Parallel and Distributed Systems</i> , Vol.2, No.4, pp.452-471, Oct. 1991.

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